+36-V, +1-A, 3.5-μV_{RMS}, RF LDO Voltage Regulator

FEATURES

- **Input Voltage Range: +3 V to +36 V**
- **Constant Output Voltage Noise vs Nominal Output Voltage (V_{OUT} = 1.4 V to 19.1 V):**
  - **3.5 μV_{RMS} (10 Hz, 100 kHz)**
  - **< 25 nV/√Hz (10 Hz, 1 MHz)**
- **Power-Supply Ripple Rejection: 80 dB (1 kHz)**
- **User-Adjustable Output via PCB Layout (No external resistors or feed-forward capacitors required): +1.4 V to +18 V**
- **Maximum Output Current: 1 A**
- **Dropout Voltage: 0.6 V at 1 A**
- **CMOS Logic Level-Compatible Enable Pin**
- **Built-In Fixed Current Limit and Thermal Shutdown**
- **Available in High Thermal Performance:**
  - **5-mm × 5-mm QFN**
- **Operating Temperature Range: –40°C to +125°C**

APPLICATIONS

- **Voltage-Controlled Oscillators (VCO)**
- **Frequency Synthesizers**
- **Test and Measurement Applications**
- **Medical Applications**
- **RX, TX, and PA Circuitry**
- **Supply Rails for Operational Amplifiers, DACs, ADCs, and Other High-Precision Analog Circuitry**
- **Audio Applications**
- **Post DC/DC Converter Regulation and Ripple Filtering**
- **Industrial Instrumentation**
- **Base Stations and Telecom Infrastructure**
- **+12-V and +24-V Industrial Buses**

DESCRIPTION

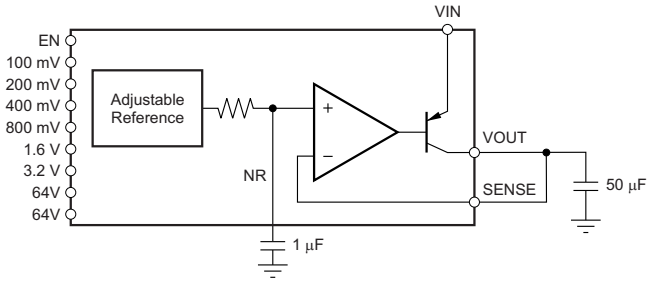
The TPS7A47 is a positive voltage (+36 V), gain-independent, ultralow-noise (3.5 μV_{RMS}) linear regulator capable of sourcing a maximum 1-A load.

In contrast with other voltage regulators, which amplify intrinsic noise as a function of output voltage, the TPS7A47 maintains a constant intrinsic noise level constant throughout the output voltage range, from 1.4 V to 19.1 V. In addition, the TPS7A47 output voltage is fully user-adjustable via the printed circuit board (PCB) layout without the need of external resistors, thus reducing overall component count.

The TPS7A47 is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry in critical applications (such as medical, RF, test, and measurement).

In addition, the TPS7A47 is ideal for post dc/dc converter regulation. By filtering out the output voltage ripple inherent to dc/dc switching conversion, maximum system performance is ensured in sensitive instrumentation, test and measurement, audio, and RF applications.

For applications where positive and negative low-noise rails are required, consider TI's TPS7A33 family of negative high voltage, ultralow noise linear regulators.



PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	OUTPUT VOLTAGE	ORERING NUMBER	TRANSPORT MEDIA, QUANTITY
TBD	TBD	TBD	TBD	TBD	TBD	TBD

(1) For the most current package and ordering information, contact your TI representative.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range, unless otherwise noted.(1)

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	IN pin to GND pin	–0.3	+36	V
	EN pin to GND pin	–0.3	+36	V
	EN pin to IN pin	–36	+0.3	V
	OUT pin to GND pin	–0.3	+36	V
	NR pin to GND pin	–0.3	+36	V
	SENSE pin to GND pin	–0.3	+36	V
	0P1V pin to GND pin	–0.3	+36	V
	0P2V pin to GND pin	–0.3	+36	V
	0P4V pin to GND pin	–0.3	+36	V
	0P8V pin to GND pin	–0.3	+36	V
	1P6V pin to GND pin	–0.3	+36	V
	3P2V pin to GND pin	–0.3	+36	V
	6P4V1 pin to GND pin	–0.3	+36	V
	6P4V2 pin to GND pin	–0.3	+36	V
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J	–40	+125	°C
	Storage, T_{stg}	–65	+150	°C
Electrostatic discharge (ESD) rating(3)	Human body model (HBM) QSS 009-105 (JESD22-A114A)		1	kV
	Charge device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

At –40°C ≤ T_J ≤ +125°C; V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or V_{IN} = 3.0 V (whichever is greater); V_{EN} = V_{IN}; I_{OUT} = 1 mA; C_{IN} =10 µF; C_{OUT} = 50 µF; C_{NR} = 1 µF; SENSE tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		3		35	V
V_{REF}	Internal reference	T_J = +25°C, V_{OUT} = V_{REF}	1.365	1.400	1.435	V
V_{OUT}	Output voltage range	V_{IN} ≥ $V_{OUT(NOM)}$ + 1.0 V	V_{REF}		19.1	V
	Nominal accuracy	T_J = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V	–1.0		1.0	%V_{OUT}
	Overall accuracy	$V_{OUT(NOM)}$ + 1.0 V ≤ V_{IN} ≤ 35 V, 1 mA ≤ I_{OUT} ≤ 1 A	–2.5		2.5	%V_{OUT}
$\Delta V_{OUT}(\Delta V_{IN})/V_{OUT(NOM)}$	Line regulation	$V_{OUT(NOM)}$ + 1.0 V ≤ V_{IN} ≤ 35 V		0.14		%V_{OUT}
$\Delta V_{OUT}(\Delta I_{OUT})/V_{OUT(NOM)}$	Load regulation	1 mA ≤ I_{OUT} ≤ 1 A		0.4		%V_{OUT}
V_{DO}	Dropout voltage	V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 0.5 A		216		mV
		V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 1 A		325	600	mV
I_{CL}	Current limit	V_{OUT} = 90% $V_{OUT(NOM)}$	1.1	1.6	2.1	A
I_{GND}	Ground pin current	I_{OUT} = 0 mA		0.36	2.0	mA
		I_{OUT} = 1 A		TBD		mA
I_{SHDN}	Shutdown supply current	V_{EN} = 0.4 V		1	3	µA
				14	100	nA
I_{EN}	Enable pin current	V_{EN} = V_{IN} = $V_{OUT(NOM)}$ + 1.0 V		0.48	1	µA
		V_{IN} = V_{EN} = 35 V		0.51	1	µA
$V_{+EN(HI)}$	Enable high-level voltage		2.0		V_{IN}	V
$V_{+EN(LO)}$	Enable low-level voltage		0.0		0.4	V
V_{NOISE}	Output noise voltage	V_{IN} = 3 V, $V_{OUT(NOM)}$ = V_{REF}, C_{OUT} = 50 µF, C_{NR} = 1 µF, BW = 10 Hz to 100 kHz		3.5		μV_{RMS}
		V_{IN} = 6.2 V, $V_{OUT(NOM)}$ = 5 V, C_{OUT} = 50 µF, C_{NR} = 1 µF, BW = 10 Hz to 100 kHz		3.5		μV_{RMS}
PSRR	Power-supply rejection ratio	V_{IN} = 6.2 V, $V_{OUT(NOM)}$ = 5 V, C_{OUT} = 50 µF, C_{NR} = 1 µF, f = 1 kHz		72		dB
T_J	Operating junction temperature		–40		+125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+170		°C
		Reset, temperature decreasing		+150		°C

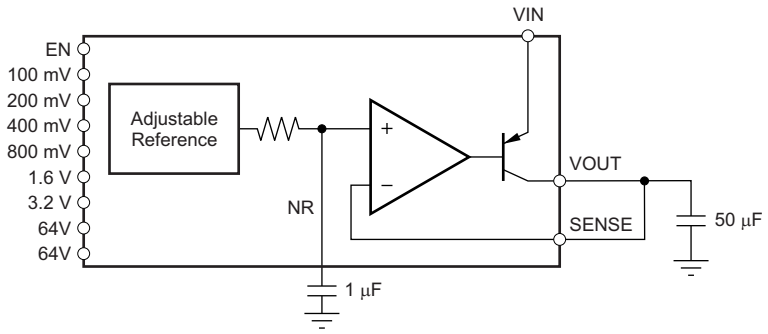
PRODUCT PREVIEW

THERMAL INFORMATION

THERMAL METRIC(1)		TPS7A47	UNITS
		TBD	
		TBD	
θ_{JA}	Junction-to-ambient thermal resistance	TBD	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	TBD	
θ_{JB}	Junction-to-board thermal resistance	TBD	
ψ_{JT}	Junction-to-top characterization parameter	TBD	
ψ_{JB}	Junction-to-board characterization parameter	TBD	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	TBD	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

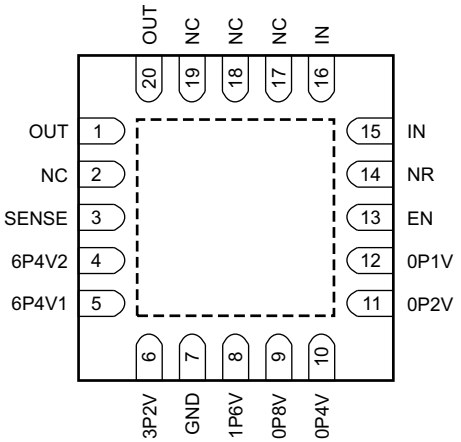
FUNCTIONAL BLOCK DIAGRAM



PRODUCT PREVIEW

PIN CONFIGURATIONS

RGW PACKAGE
5-mm × 5-mm QFN-20
(TOP VIEW)



PIN DESCRIPTIONS

PIN		
NAME	**NO.**	**DESCRIPTION**
0P1V	12	When connected to GND, this pin adds 0.1 V to the regulator nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P2V	11	When connected to GND, this pin adds 0.2 V to the regulator nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P4V	10	When connected to GND, this pin adds 0.4 V to the regulator nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P8V	9	When connected to GND, this pin adds 0.8 V to the regulator nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
1P6V	8	When connected to GND, this pin adds 1.6 V to the regulator nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
3P2V	6	When connected to GND, this pin adds 3.2 V to the regulator nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
6P4V1	5	When connected to GND, this pin adds 6.4 V to the regulator nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
6P4V2	4	When connected to GND, this pin adds 6.4 V to the regulator nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
EN	13	This pin turns the regulator on and off.
GND	7	Ground
IN	15, 16	Input supply. A capacitor greater than or equal to 1 µF must be tied from this pin to ground to assure stability. It is recommended to connect a 10-µF capacitor from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed-circuit-board (PCB) layout, especially when long input traces or high source impedances are encountered.
NC	2, 17-19	This pin can be left open or tied to any voltage between GND and IN.
NR	14	Noise reduction pin. When a capacitor is connected from this pin to GND, RMS noise can be reduced to very low levels. It is required to connect a 1-µF capacitor from NR to GND (as close to the device as possible) to ensure stability and maximize ac performance.
OUT	1, 20	Regulator output. A capacitor greater than or equal to 10 µF must be tied from this pin to ground to assure stability. It is highly recommended to connect a 47-µF ceramic output capacitor from OUT to GND (as close to the device as possible) to maximize ac performance.
SENSE	3	Control-loop error amplifier input. This pin must be connected to OUT. It is recommended to connect to OUT at the point of load to maximize accuracy.

PRODUCT PREVIEW

TYPICAL APPLICATION CIRCUIT

Output voltage is set by grounding the appropriate control pins, as shown in Figure 1. When grounded, all control pins add a specific voltage on top of the internal reference voltage (V_{REF} = 1.4 V). For example, when grounding pins 0P1V, 0P2V, and 1P6V, the voltage values 0.1 V, 0.2 V, and 1.6 V are added to the 1.4-V internal reference voltage for $V_{OUT(NOM)}$ equal to 3.3 V, as described in Equation 1.

$$V_{OUT(NOM)} = V_{REF} + 0.1\ V + 0.2\ V + 1.6\ V = 1.4\ V + 0.1\ V + 0.2\ V + 1.6\ V = 3.3\ V \quad (1)$$

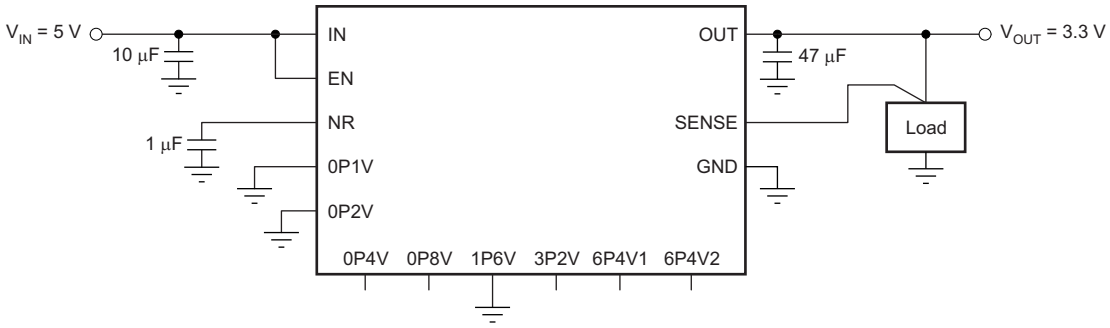


Figure 1. Maximize PSRR Performance and Minimize RMS Noise (3.5 μV_{RMS})

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS7A4700RGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS7A4700RGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

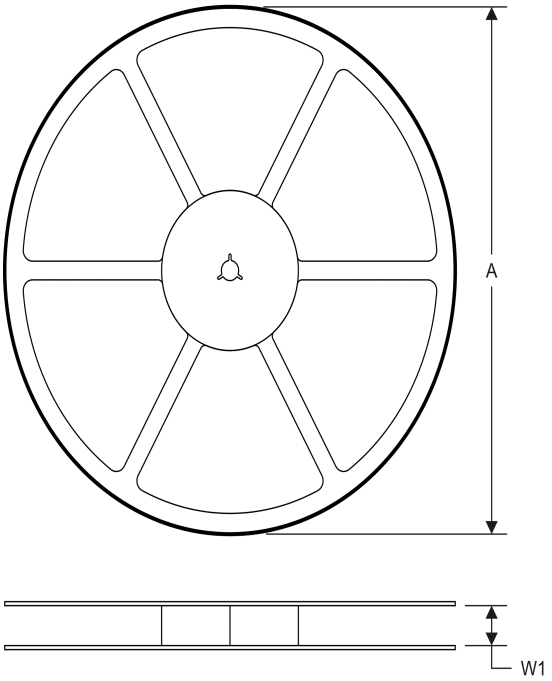
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

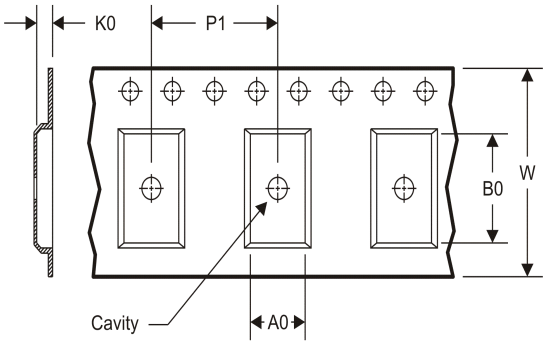
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



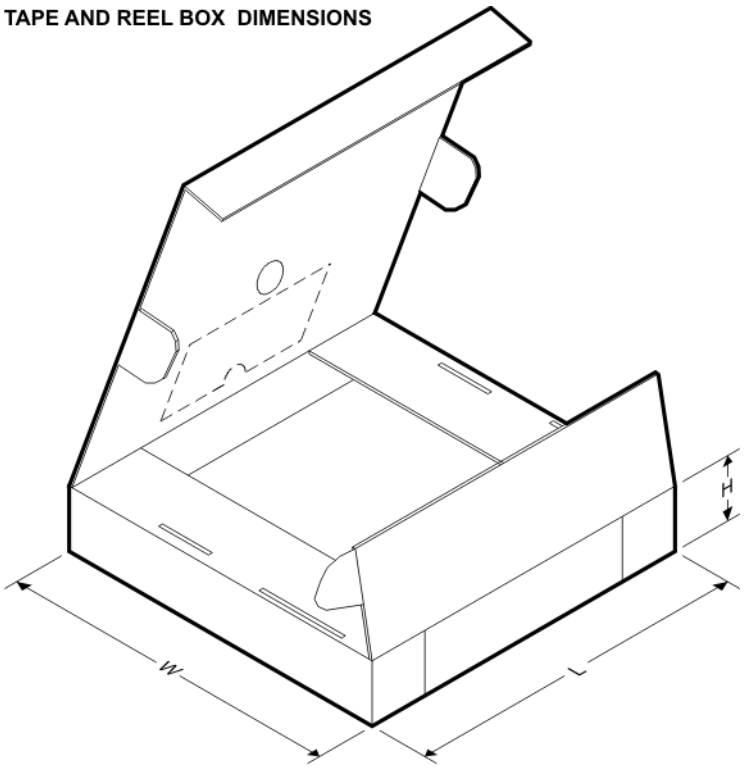
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4700RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS7A4700RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

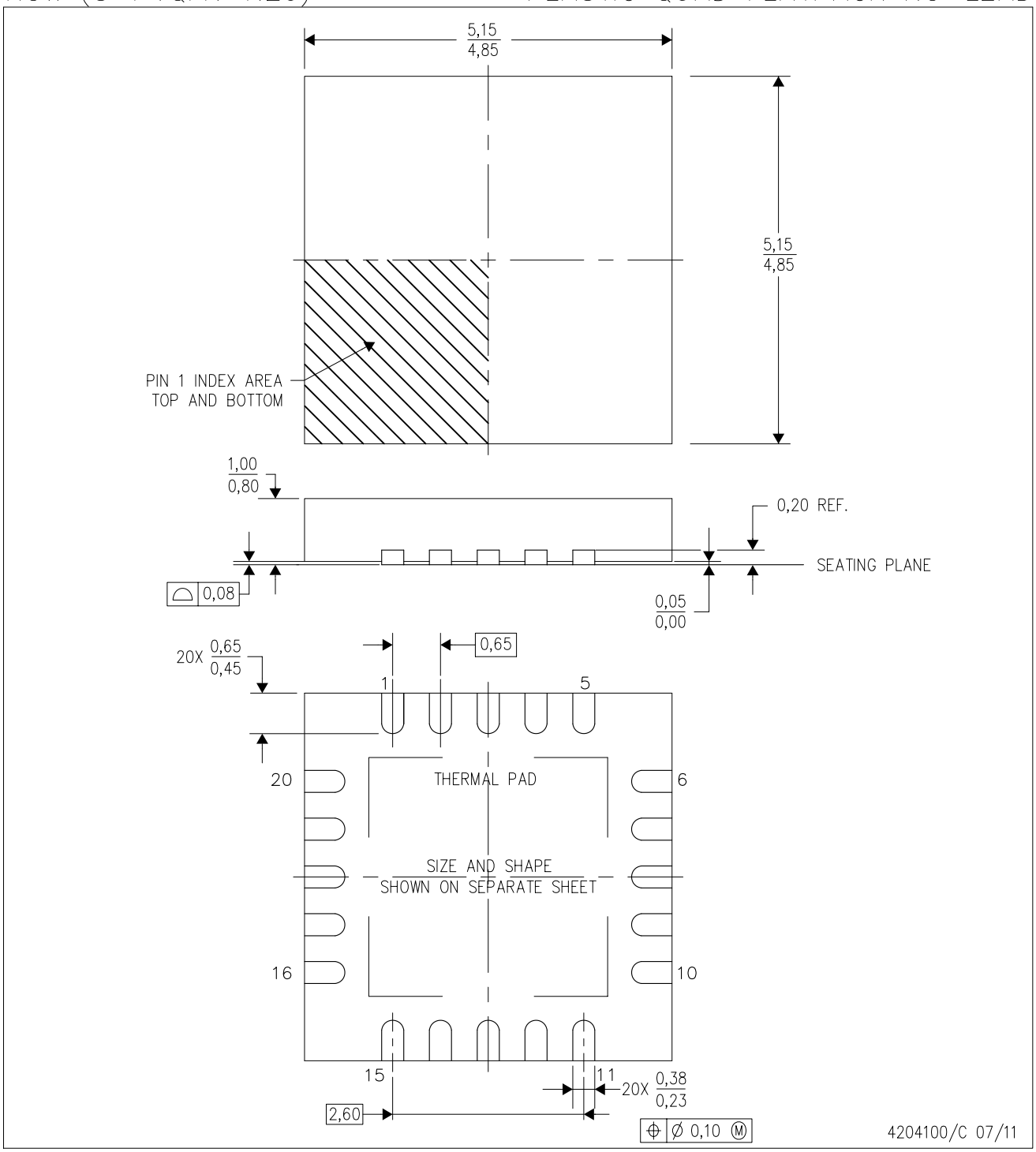
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4700RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS7A4700RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

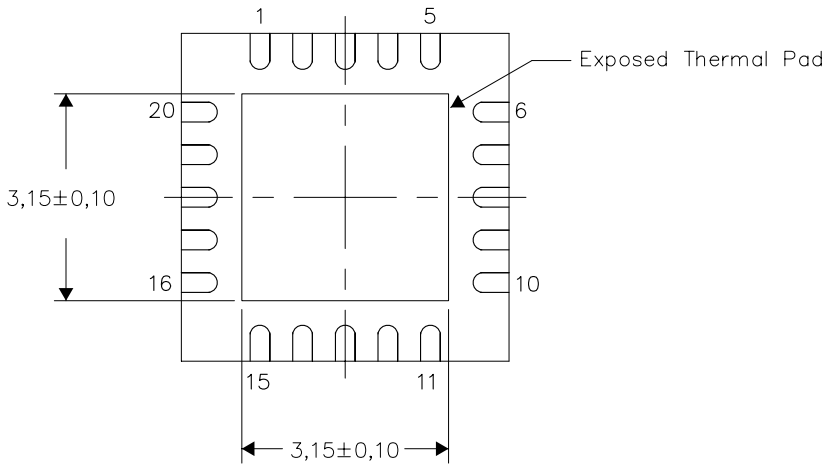
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



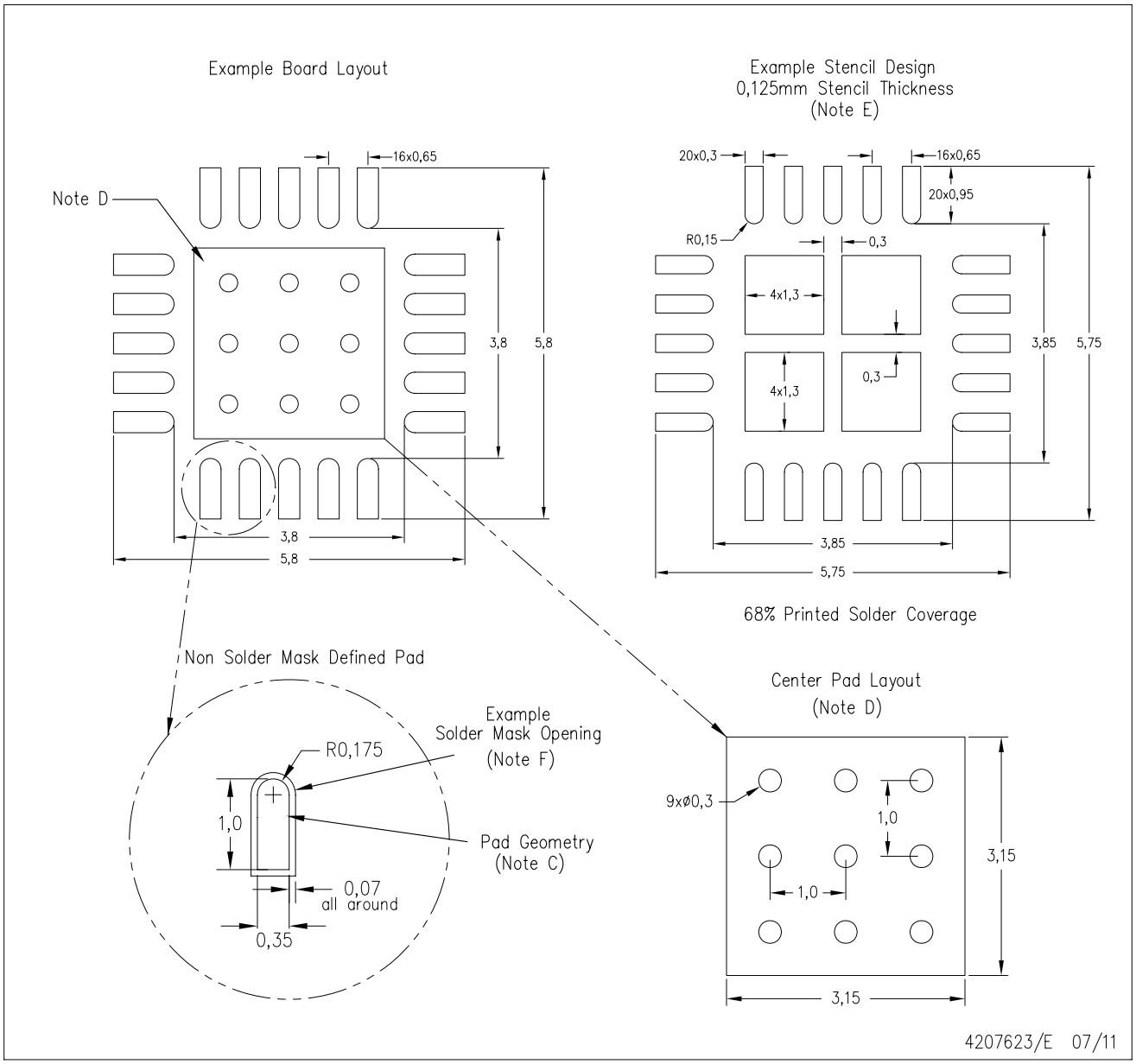
Bottom View

Exposed Thermal Pad Dimensions

4206352–2/J 07/11

NOTE: All linear dimensions are in millimeters

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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